Paper from Proceeding of the National Conference "Science in Media 2012" Organized by YMCA University of Science and Technology, Faridabad, Haryana (India) December 3rd -4th 2012 Published by IJMRS's International Journal of Engineering Sciences, ISSN (Online): 2277-9698
www.ijmrs.com

Analytical Comparison of different 1-Bit full adder's scheme for 250nm CMOS technology

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***Abstract*—A full adder is one of the most commonly used digital circuit component in any digital system design, over the years many improvements have been suggested to modify the architecture of a full adder. So far, the full adder of 10-T (transistors) architecture are considered as the most optimized design for performance and area. In this paper, 5 different types of 1 bit full adder namely 28T, 10T, 14T, Modified 14T and 12T adder is compared based on the basis of different parameters. The simulation has been carried out with properly defined simulation runs on a SPICE environment using a 0.25µm process. The results may be differ from those previously published, both for the more realistic simulations carried out and the more appropriate figure of merit used. The main objective is to find out Delay, Power and Power delay product (PDP) of different full adders scheme and carry out the comparison.**

***Index Terms*—CMOS Circuit, VLSI, Full adder, SPICE, PDP**

I. Introduction

With the continuously increasing IC complexity and number of transistors, circuit power consumption is growing as well. Technology trends show that circuit delay is scaling down by 30%, performance and transistor density are doubled approximately every two years, and the transistor's threshold voltage is reduced by almost 15% every generation[1]. All of these technology trends lead to higher and higher power consumption in circuits. Higher power consumptions raises IC temperature and directly affect battery life in portable devices as it causes more current to be withdrawn from the power supply. A higher temperature directly affects circuit operation and reliability, as a result complicated cooling and packaging techniques are required.

Full adders are fundamental units in various circuits, especially in circuits used for performing arithmetic operations such as compressors, comparators, parity checkers and so on. There are several issues related to the full adders. Some of them are, power consumption, performance, area, noise immunity and regularity and good driving ability. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area [2,5,6,8]. Some of them has threshold loss problem that cause non-full swing outputs, low speed and low noise immunity[3]. However, usually they have less power consumption in comparison to full adders with full swing outputs. Not full swing full adders are useful in building up larger circuits as multiple bit input adders and multipliers. With the increasing demand for battery-operated portable applications such as cell phones, PDAs and laptop computers, as well as low-intensity applications such as distributed sensor networks, the need for power sensitive design has grown significantly.

It has been shown that reducing the supply voltage is the most direct means of reducing dissipated power [4,6], and operating CMOS devices in the sub threshold region is considered to be the most energy-efficient solution for low-performance applications [5]. These papers have investigated different approaches for realizing adders using CMOS technology; each has its own pros and cons. To summarize, some performance criteria are considered in the design and evaluation of adder cells. After introducing a novel design methodology, a high-speed CMOS 1-bit adder cells is presented .The paper is organized as follows: Section II explores power consumption in digital CMOS, Section III explores conventional CMOS design style, 10T SERF adder,14T full adder, modified 14T full adder,12T full adder. Section IV shows the simulation results in a 0.25-µm standard CMOS process technology, and finally some conclusions are given.

II. POWER CONSUMPTION IN DIGITAL CMOS

The average power dissipated in a generic digital CMOS gate is given by [4], [5]:

$$\mathbf{P}avg = P_{dynamic} + P_{short\text{-}circuit} + P_{static}$$

$$= V_{dd} \cdot F_{clk} \cdot \Sigma (Vi_{swing} \cdot Ci_{load} \cdot \alpha_i) + \Sigma V_{dd} \cdot Ii_{sc} + V_{dd} \cdot I_l \quad (1)$$

Where f_{clk} denotes the system clock frequency, *Vi* swing is the voltage swing at node *i* (ideally equal to V_{DD}), C_i load is the load capacitance at node *i*, α_i is the activity factor at node *i*, and I_i sc and I_l are the short circuit and leakage currents, respectively.

When operating CMOS devices in the subthreshold region, the power supply voltage is kept lower than the absolute of the devices' threshold voltage. This ensures that the transistor channel is never fully inverted, but is operated in weak or moderate inversion while the transistor is in its 'on' state. According to [8], subthreshold logic gates have a near ideal voltage transfer characteristic, due to the exponential I-V relationship. We model the I-V relationship of the saturated device in weak inversion through the EKV model [9]:

$$Isub=I_s\left[e^{\frac{Vg - Vto - nVs}{nUt}}\right] \quad Vds > 4.Ut \qquad (2)$$

Where I_S is the specific current defined by the model:

$$Is = 2\eta\, \eta_n(p)\, .C_{ox}.W/L.Ut^2 \qquad (3)$$

Note that all potentials are referred to the local substrate. U_t is the thermal voltage, $\eta_n(p)$ is the carrier mobility for n or p channel devices, C_{ox} is the oxide capacitance, and W and L are the effective width and length of the channel.

III CMOS DESIGN STYLE

Conventional CMOS Style

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B and C_{in}) and two 1-bit outputs (*sum* and *carry*). The relations between the inputs and the outputs are expressed as:

sum = (a xor b) xor c (4)
carry = a. b+ c(a xor b) (5)

The above Boolean expressions may be rearranged as:
sum = c(a+b+c) + a.b.c (6)
carry = a.b+(a+ b)

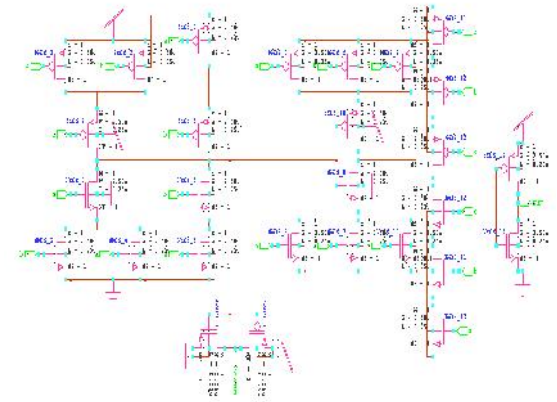


Fig 1 schematic circuit of 28T full adder

In the 1-bit conventional CMOS full adder cell is shown in Fig. 1. The 1-bit full adder cell has 28 transistors.

10T SERF ADDER

As an initial step toward designing low power arithmetic circuit modules Static Energy Recovery Full adder (SERF) cell module [8] illustrated in Figure 2. The cell uses only 10 transistors and it does not need inverted inputs. The design was inspired by the XNOR gate full adder design. In non-energy recovery design the charge applied to the load capacitance during logic level high is drained to ground during the logic level low. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption, removing the P_{sc} variable (product of I_{sc} and voltage) from the total power equation.

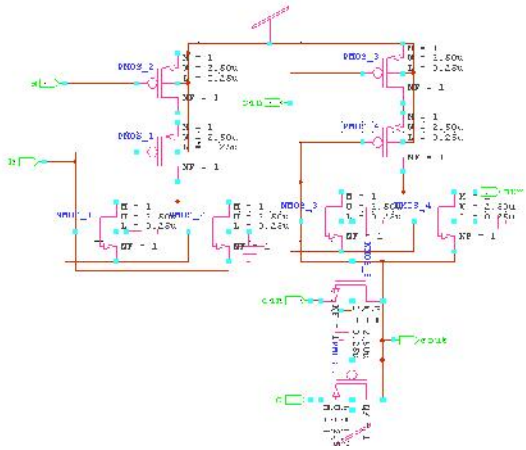


Fig-2. Schematic diagram of 10T SERF adder

14T FULL ADDER

As the name implies, uses 14 Transistors [7] to realize the adder function (See Fig.3). The 14T full adder cell, like the transmission function full adder cell, implements the complementary pass logic to drive the load. Though SERF adder [4] consumes less power it suffers from threshold loss problem as both sum and carry are generated from pass transistor logic so need for the 14T to improve threshold loss problem.

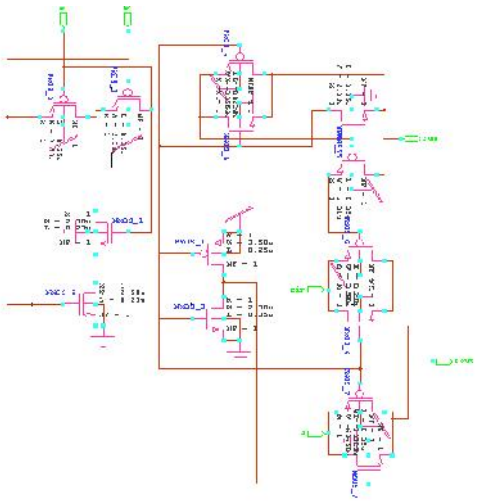
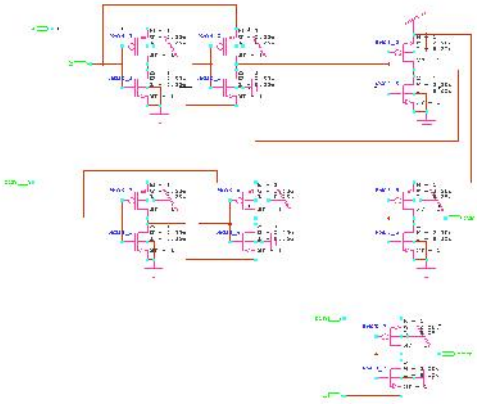


Fig.3 schematic diagram of 14T full adder

Modified 14T 1-bit full adder

The new improved 14T adder cell requires only 14 transistors to realize the adder function shown in Fig.4. It produces the better result in threshold loss, speed and power

by sacrificing four extra transistors per adder cell. Even though the transistor count increases by four per adder cell, it reduces the threshold loss problem, which exists in the SERF by inserting the inverter between XOR Gate outputs to form XNOR gate



In the modified 14T adder has a four transistor xor structure, a four transistor xnor structure and an inverter. Figure.4 shows the xor and xnor structures used in modified 14T adder. The first xor structure gives a good logic '0' as it has a ground and the xnor structure gives a good logic '1' as it has a VDD. The circuit diagram of modified 14T full adder is shown in Figure. The sum and carry are generated as per the equations given below.

$$sum = (A \Theta B) \quad C + (A \oplus B) \quad C \qquad (7)$$

$$carry = (A \oplus B) \quad C + (A \Theta B) \quad A \qquad (8)$$

The sum output logic is pass transistor logic and while the carry output is transmission gate logic. The difference in the full adder structure of the existing 14T Full adder and modified structure [7] is the implementation of the sum equation, which results in the better performance of modified 14T full adder.

V 12T full adder

A full adder is one of the most commonly used digit circuit component, many improvements have been made to refine the architecture of a full adder. So far, the full adders of 10-T (transistors) architecture are considered as the most balanced design regarding performance and area. However, the era of deep sub-micron CMOS process has come which makes the traditional 10-T designs no applicable in the mentioned CMOS process, the 12-T full adder is better than the some prior designs which makes it a better alternative In order to generate correct outputs, 3 steps are adopted. They are:

1) Provide full swing MID signal: We have add an inverting buffer at the output of the XOR block. This will generate a full swing MID signal.

2) Modify SUM block: Since the improper MID signals are now inverted, the SUM blocks are modified accordingly to generate correct SUM outputs.

3) Modify Cout block: The COUT blocks are also modified to generate correct COUT output.

The refined full adders are shown in Fig.5. With 2 extra transistors as well as the improvements above, we manage to provide correct outputs in TSMC 0.25 µm

CMOS process.

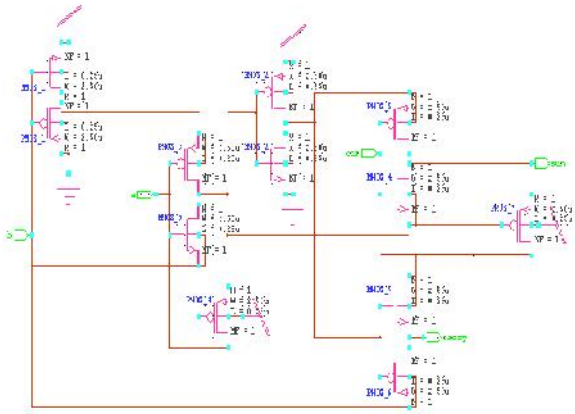


Fig-5 Systematic diagram of 12T full adder

IV Simulation results

Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, CMOS devices are best known for low power consumption. Hence there is a simulation of different full adder scheme. The simulation is done on the 250nm technology. After simulation the main parameters that have calculated is Power, Delay and the power delay Product (PDP).

Each one-bit full adder has been analyzed in terms of propagation delay, average power dissipation and their product. The propagation delay has been measured as the time interval between the time the input signal takes to reach 50% of its logic swing and the time the output takes to reach the same value (for the case of differential input and output, we considered the worst value among the outputs and its complemented value). The power dissipation has been evaluated by averaging the power flowing into the full adder.

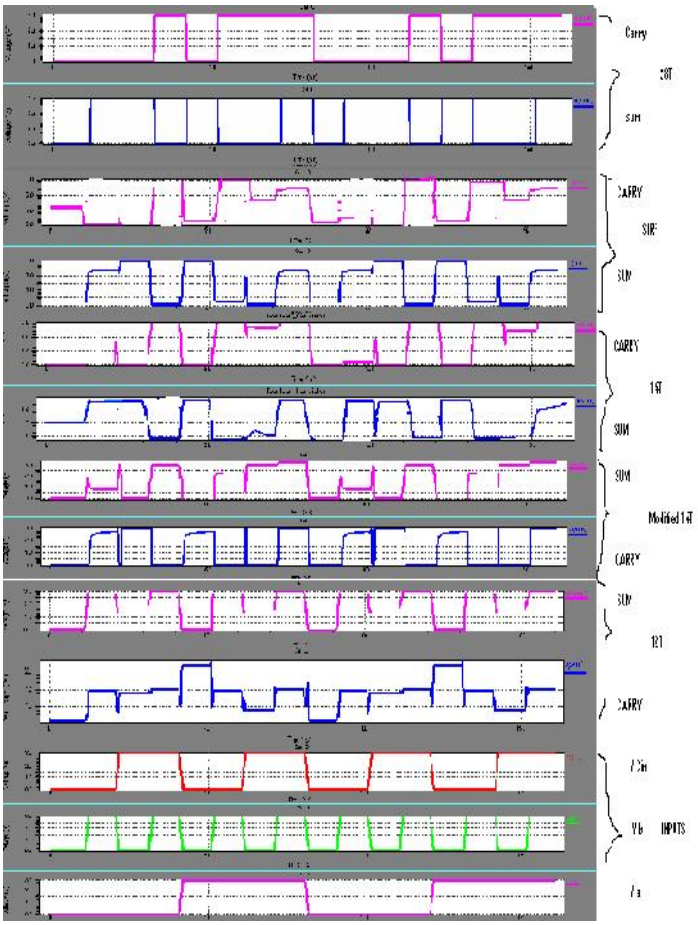
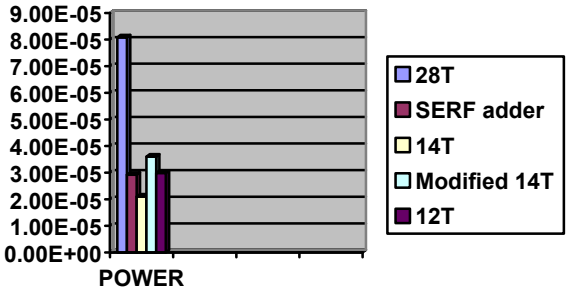
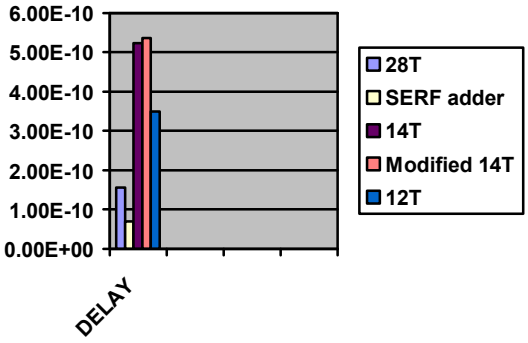


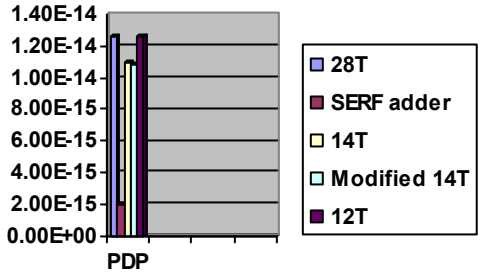
Fig -6 Simulation results of different full adder scheme.

The comparison of different full adder for various parameter like Delay , Power and Power delay product is in the Table -I .

S. No..	Adder	Delay	Power	Power delay product (PDP)
1	28T	1.56E-10	8.08E-05	1.26E-14
2	SERF adder	6.99E-11	2.92E-05	2.04E-15
3	14T	5.24E-10	2.10E-05	1.10E-14
4	Modified 14T	7.37E-10	2.99E-05	2.20E-14
5	12T	3.49E-10	3.60E-05	1.26E-14







V CONCLUSION

In this paper different full adder circuits are compared to calculate the various parameters like power consumption, delay and power delay product. According to simulations results, the power consumption is minimum in case of SERF adder. The delay is less in 28T but the problem is of power consumption, so it can be used where there is need of high speed and the power consumptions is secondary matter. In case of modified 14T the output is much better than the 14T. The 12T full adder also having some better results as the swing in the circuit is reduced. The results also show that many of then can be suitable for ultra low power applications.

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