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A Review of Various Techniques for Protection of IC Circuit from Electro Static Discharge

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Abstract-- This paper review various techniques used these days to remove errors which arise because of Electro-static Discharge (ESD) in proper working of IC circuit. According to an estimate, ESD accounts for more than 40% of total failure of integrated circuits. The sources of ESD, causes and types of failure are briefly discussed in this paper. The three mostly used devices and their use in protecting internal circuit from ESD with some of the possible circuit design has been explained. Starting from diode based protection circuit design to more complex MOSFET based two stages ESD protection design and substrate triggered Field Oxide Device (FOD) design, are reviewed and compared. The possible protection circuit design for output circuit is also discussed.

Key word-- ESD, FOD, ggNMOS, MOSFET.

I. INTRODUCTION

The electro static charge (ESD) is sudden transfer of charge between two objects at different potentials, so it is the charge balancing process between two objects. ESD is a transient discharge of static charge that arises from either human handling, during manufacturing, testing, handling and assembly of integrated circuits (ICs). This unintentional charge transfer may generate large voltages (100V to 10 kV)[2] due to the small size and capacitance of the integrated devices. These large voltages can result in high currents through the devices that may cause malfunctioning or even permanent damage to the circuit. The energy dissipated and damage made is mainly due to current in ICs during discharge.

Most ESD damage is thermally initiated process in the form of device / interconnect burn-out or oxide break-down. The basic phenomenon is that sufficient heat is generated in a small volume significantly faster than it can be removed, leading to a temperature rise beyond the limit of the IC circuit.

Other than these effects ESD can cause errors in safe operating limits as:

PN-junction may melt.

- Void formation in gate oxide.
- Metal interconnects / vias may melt or vaporization, leading to shorts/open circuit.

II. PRINCIPLE SOURCES OF ESD IN IC'S

A. Human Factors [1]

A person working on a synthetic floor can accumulate up to 20 kV. This voltage is discharged when the person touches an object that is sufficiently at ground as the circuit completed. Charge exchange occurs between the person and the object in very short time duration (10 ns - 100 ns). The discharging current is approximately 1A - 10A, depending upon the time constant. This is the main factor in ESD to cause IC circuit damage.

B. Application of Test and Handling Systems

Equipment can accumulate static charge due to improper grounding. The charge is transmitted through ICs when it is picked up for placement in test sockets during the testing of the circuit.

C. Self charged IC

Sometimes IC becomes charged during transport or by the contact with charged object. ICs remain charged until they come into contact with a grounded surface (large metal plates /test sockets). Charge is discharged through the pins of ICs. Large currents in the internal circuit can result in high voltage inside the devices, which can cause damage to thin dielectrics and insulators as large current would flow through them.

III. FAILURE

A. Types of failure

Hard failure: Physical destruction of device so that it is no longer works properly.

Soft failure: Temporary change in logic functions for short span of time.

Latent failure: Development of stresses in device and leading to its failure after some period of its use.

B. Causes of failure

- Interconnect lines are finer thus more susceptible to fusing.
- Junction depths are shallower thus more prone to degradation.
- Low oxide thickness breaks at lower breakdown voltages.

IV. ESD PROTECTION DEVICES

A. Resistor [1]

N-well resistors exhibit a large resistance in the saturation region. N-well resistors in the saturation region can be used as current-limiting devices for ESD protection by limiting the amount of ESD discharging current.

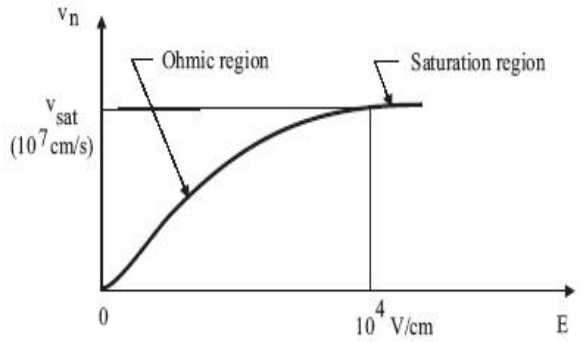

Figure 1: Saturation Velocity.

At high voltages, the velocity of free electrons saturates due to the increasing collision with silicon lattices. As a result, the current through n-well resistors remains nearly constant regardless of voltage increase

B. Diodes [1]

When forward-biased, diodes can sustain a large current with a small device dimension. The ON resistance of PN diode at high current levels is much lower. Reverse biased diodes have high resistance so they are not suitable ESD current shunt. Heating in reverse biased diode is high than forward biased diode due to presence of high electric field.

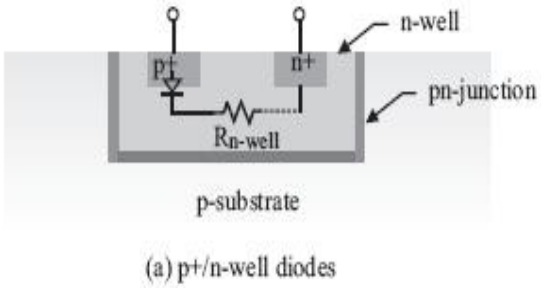

Figure 2: Diode cross-section.

C. MOSFET [1]

MOSFET can also be used as the protection device of the circuit from ESD. The main design parameters of NMOS are (i) channel length, (ii) drain contact-to-gate spacing, and (iii) device width. The source contact-to-gate spacing is not critical and is kept at its minimum design value.

i) The minimum channel length is good for efficient turn-on but the punch-through limit will be reduced.
ii) Drain contact-to-gate spacing affects the resistance of ballast resistors. For silicide processes, the minimum drain contact-to-gate spacing is used.
iii) Device width determines the maximum current that the device can conduct.

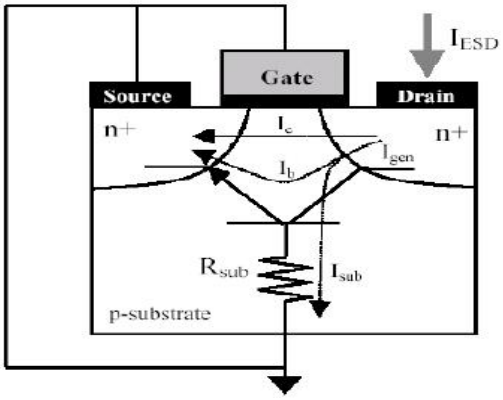

Figure 3: Typical operation of NMOS.

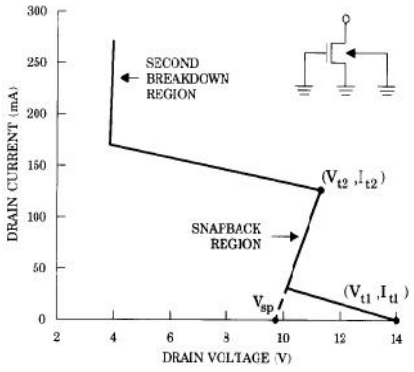

Figure 4: V-I characteristics of MOSFET under ESD.

During a ESD strike (shown in Figure 3) the PN-junction at the drain is reverse biased and as the ESD pulse increases it undergoes an avalanche breakdown which results in very small conduction in the device as shown by V_{t1}, I_{t1} in Figure 4. Holes flow to the substrate thus substrate potential increases, and this potential increases till source and substrate junction is forward biased at V_{sp} then NMOS moves in snapback region as shown in Figure 4. This snapback mode results in turning ON of parasitic BJT, thus ESD current flows from the collector the (drain of NMOS) to the emitter (the source of NMOS that is connected to the ground) as shown in figure 3. In snapback region there is small variation of voltage but very sharp increase of current this rise is upto holding voltage V_{t2}, I_{t2} as shown in Figure 4. Upto, which ESD stress at the drain of the NMOS transistor (PAD), is released.

The ESD stress should be released upto V_{t2}, I_{t2} as shown in Figure 4, because after this second breakdown of device takes place, the device fails at that point and would not be workable after this point.

The dimensions of ESD NMOS should be large enough to handle large ESD currents, also multiple fingers structure is used to implement ESD NMOS because for them ESD pulse flows through many devices thus averting damage of any device due to ESD stress. In order to achieve this gate-coupled NMOS is used because V_{t1} is lower than V_{t2}, hence there is uniform triggering of all NMOS fingers.

D. Features of ESD Protection Circuits

- An ESD protection circuit should provide a low-impedance path from input pads to the ground during an ESD strike to release the static charge accumulated on the pads.
- Clamp the voltage of the pads at a level that is below the dielectric breakdown voltage of thin transistors during an ESD strike.
- Provide very high impedance and a low capacitance during normal operation such that it has a little effect on the operation of the protected circuits.

IV. SIMPLIFIED ESD PROTECTION CIRCUITS [1]

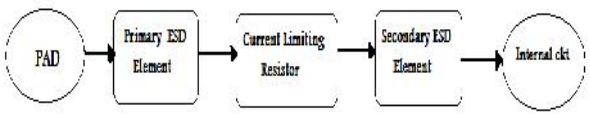

Figure 5: Block diagram of ESD Protection circuit.

- Primary ESD Element: It conducts more in bulk thus results in higher power dissipation capability. Primary ESD protection elements have large width and need more time to turn on.
- Current limiting resistor: It provides voltage drop required to activate primary, limit the current flowing into the internal circuits and withstand some ESD voltage so that the secondary protection circuit will not be damaged in an ESD strike.
- Secondary device: It is triggered at voltage below the breakdown voltage of input transistor. Since, it is not required to carry large currents they serve to limit the voltage at the circuit being protected until the primary ESD protection devices are fully operational. These devices have smaller width.
- The effectiveness of the primary ESD protection devices is determined by the secondary protection stage. Due to the small dimensions, the secondary protection devices start operating before the primary protection devices are activated. It is critical to ensure that the operation of the primary protection devices is activated before the secondary protection devices enter their thermal breakdown so that the secondary ESD protection devices will not be destroyed by ESD stress.

V. INPUT CIRCUIT PROTECTION

A. *Using diode [1]*

Large area diodes D1 and D2 are used to dissipate large current as shown in Figure 6, the ESD protection circuitry need to be triggered before gate oxide is damaged, in order to overcome this issue two small area diodes D3 and D4 are used. Now if the positive ESD pulse is applied. When time equivalent to product of junction capacitance of diode D3 and current limiting resistor has lapsed then D3 starts conducting in forward mode, in the meantime current flow through resistor is increasing and this result, in the increase of potential drop at node of D1, D2 and resistor.

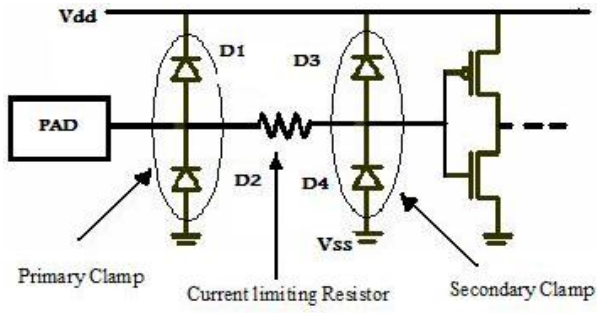

Figure 6: ESD Protection circuit using diodes.

Thus, rise of potential at this node leads to turning ON of diode D1. Since, D1 is very large area diode so it releases whole ESD stress. Hence, both objectives are achieved.

B. Using MOSFET

1) Two-stage ESD protection circuit [4]:

To protect the thinner gate oxide of the input stage in CMOS ICs under all ESD stress conditions, a traditional two-stage ESD protection circuit for the digital input pin is shown in Figure 7. A gate-grounded short-channel NMOS is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. To provide a high ESD protection level, a field-oxide device (FOD) is often used as the main discharge element in the primary protection stage to discharge ESD current. Between the primary and secondary stages, a resistor R is added to limit ESD current flowing through the short-channel NMOS in the secondary stage. The primary ESD clamp device must be triggered on to discharge ESD current before the gate-grounded NMOS (gg NMOS) [4] in the secondary stage is damaged by the overstress ESD current. If the primary ESD clamp device has a high turn-on voltage, the resistance of R should be large enough, even on the order of kilo ohms. Under the positive-to- and negative-to- ESD conditions, the ESD current can be discharged through the FOD and gg NMOS devices.

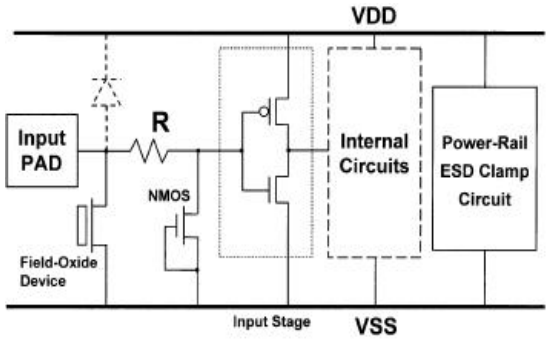

Figure 7: Traditional input ESD protection circuit for digital input pin in CMOS IC's.

However, in the mixed-voltage situation, the diode or PMOS connected from the pad to V_{DD} power line is forbidden by the normal circuit operation with a high-voltage input signal. Without the diode or PMOS connected from the pad to V_{DD}, the positive ESD stresses are still discharged from the pad to power line and then conducted through the power-rail ESD clamp circuit to the grounded pin. The efficient power-rail ESD clamp circuit is important under such ESD stress conditions to bypass ESD current away from the internal circuits.

The ESD protection device must be drawn with larger device dimensions, which has often been realized in layout with multiple fingers to reduce the total silicon area. But, during ESD stress, the multiple fingers of the ESD protection MOSFET cannot be uniformly turned on. Only several fingers of the MOSFET are turned on and, therefore, damaged by ESD. This often causes a low ESD level in the ESD protection circuit, even if the MOSFET has been drawn with a large device dimension. To efficiently improve the turn-on uniformity among those multiple fingers, the gate-driven design increase ESD robustness of the large-device-dimension NMOS. The gate-driven design causes ESD current to discharge mainly through the surface channel of the NMOS therefore the NMOS is easily burned out by ESD energy. To avoid the sudden degradation on ESD level of the gate-driven devices, the substrate triggered design can be used to improve ESD robustness of the ESD protection devices.

2) Substrate triggered design [3]:

The input ESD protection circuit with the substrate-triggered design is shown in Figure 8. This input ESD protection circuit is combined with a short-channel gate-grounded NMOS (Mn1), a resistor (R), and a FOD.

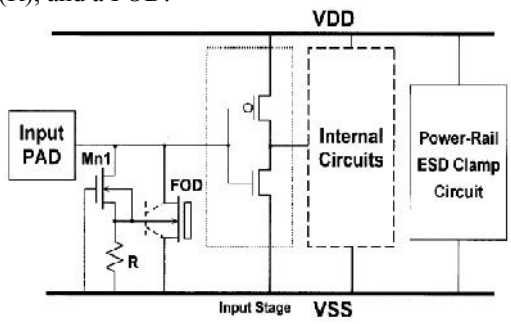

Figure 8: ESD protection circuit with substrate-triggered FOD to protect the input stage.

During ESD stress, the short-channel gate-grounded NMOS with a lower snapback breakdown voltage can be more quickly triggered on than the FOD with a higher breakdown voltage. Both the source and the substrate of the gate-grounded NMOS is connected to the substrate of the FOD to form a trigger path to the base of the parasitic lateral bipolar junction transistor (LBJT), which is shown by the dashed line beside the FOD in Figure 8. The collector/emitter of the parasitic LBJT is formed with the drain/source of the FOD and the base formed from the substrate of the FOD. To effectively trigger on this parasitic LBJT, a suitable voltage is applied on the resistance R to turn on the base–emitter junction of parasitic LBJT during ESD stress. This method works for both positive and negative ESD stresses.

During positive or negative ESD stress conditions, the ESD current is still discharged from the pad. A turn-on efficient power-rail ESD clamp circuit should be included in the chip to provide overall ESD protection for the input pin. Some of the research paper discuss more efficient use of this techniques for RF based circuits [5]. So in the circuits which are ultra sensitive part of the IC or in advance technologies these circuits techniques are used and preferred.

3) Substrate-triggered design Vs Two stage protection Design"

By using the substrate-triggered design, the FOD in Figure 8 can be uniformly turned on to sustain higher ESD levels than the traditional two stage protection design in Figure 7, under the positive ESD stress conditions. The two-stage ESD protection design may provide high ESD protection levels for the digital input pins, but because the large series resistance and the junction capacitance of the ESD clamp devices cause a long *RC* delay to the input signal, such a traditional design is not suitable for analog pins[4]. For current-mode input signals or high-frequency applications, the series resistance between the input pad and input stage is neglected. The traditional two-stage ESD protection design in Figure 7 is not suitable for analog applications. On the other hand, the substrate-triggered ESD protection circuit without series resistance, as that shown in Figure 8, can provide lower triggered voltage to effectively protect the thin gate oxide of the input stage. It is, therefore, more suitable for analog circuit applications.

C. Output Protection [3]

For the protection of output circuit, additional protection circuitry is not required. It simply can be done by using CMOS as shown in Figure 9. The CMOS used in output stage itself acts as ESD protection circuit. When positive ESD occurs then PMOS (M1) drain substrate junction is forward biased and ESD pulse gets path to flow through V_{DD}.

Similarly when negative ESD occurs then in NMOS (M2) drain substrate junction is forward biased and ESD pulse gets path to flow through V_{SS}, but for M2 we also use diode as additional protection device connected between V_{SS} and pad. We use diode for M2 because width of M1 is 2 to 3 times more than M2 so it can effectively pass ESD pulse without any damage to it whereas there are chances of M2 to get damaged.

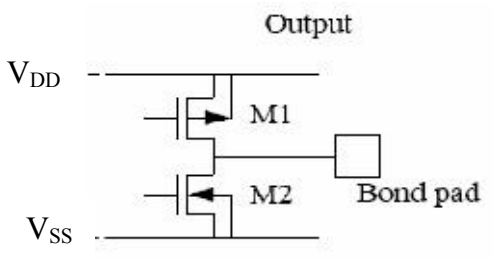

Figure 9: Output Protection using CMOS.

V. CONCLUSION

In this paper we have discussed various methods to protect the circuit from ESD. Traditional two stage design and substrate triggered FOD are also compared. The best method can be applied by taking the actual circuit into consideration i.e. we can not apply two stage design in analog circuit as it would causes input signal to delay in normal operation whereas substrate triggered FOD would protect the circuit effectively. So it important to protect the IC circuit form ESD with right design techniques, otherwise the normal operation of the circuit would be affected.

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